Design of Reconfigurable Digital IF Filter with Low Complexity

Base Paper Abstract:

Due to limited frequency resources, new services are being applied to the existing frequencies, and service providers are allocating some of the existing frequencies for newly enhanced mobile communications. Because of this frequency environment, repeater and base station systems for mobile communications are becoming more complicated, and frequency interference caused by multiple bands and services is getting worse. Therefore, a heterodyne receiver using IF filters with high selectivity has been used to minimize the interference between frequencies. However, repeater and base station systems in mobile communications employing fixed IF filters cannot actively cope with the usage of multiple frequency bands, the application of various services, and frequency recycling. Therefore, this brief proposes a reconfigurable digital IF filter with variable center frequency and bandwidth while achieving high selectivity as existing IF filters. The center frequency of filter can vary from 10MHz to 62.5MHz, and the filter bandwidth can be selective to one of 10MHz, 15MHz, and 20MHz. The proposed digital filter also reduces the complexity of adders and multipliers by 38.81% and 41.57%, respectively, compared to an existing digital filter by using a filter bank and a multi stage structure. This digital IF filter is fabricated on a 130-nm CMOS process and occupies 5.90 mm2.

Enhancement of this Project:

- To Design a reconfigurable Digital IF Filter with variable center frequency and bandwidth.
- The centre frequency can be varied from the 500MHZ to 1GHZ and filter bandwidth can be selective to one of 10MHZ, 15MHZ and 20MHZ frequency level.

Proposed Title:

- **Design of Low Complexity and Efficient Reconfigurable Digital IF Filter using Multi Stage Filter Bank.**

Proposed Abstract:

Due to limited frequency resources, new services are being applied to the existing frequencies, and service providers are allocating some of the existing frequencies for newly enhanced mobile communications. Because of this frequency environment, repeater and base station systems for mobile communications are becoming more complicated, and frequency interference caused by multiple bands and services is getting worse. The IF (Intermediate Frequency) Filters with high selectivity is used to reduce the interference between the different frequency range. Therefore, the heterodyne receivers uses the IF filter. In mobile communication the repeaters and the base station cannot actively cope because, it has fixed frequency range. Therefore, this paper proposes the new design concept of low complexity and efficient reconfigurable digital IF filters using multi stage filter bank. The multi stage filter bank of the proposed digital IF filters lowering the sample rate in order to reduce the hardware complexity. The existing system of digital IF filters uses the concept of SAW(surface acoustic wave) IF filter, it has high frequency stability and selectivity but, it does not have variable centre frequency. The SAW IF filters has the fixed frequency level only. Therefore the proposed system of digital IF filters uses the concept of multi stage filter bank in order to reduces the hardware complexity and better performance. The proposed digital IF filters uses the different centre frequency from the range of 500MHZ to 1GHZ and filter bandwidth can be selective to one of 10MHZ, 15MHZ and 20MHZ frequency level. The proposed digital IF filter reduces the complexity of adders and multipliers. Finally, The Digital IF filter using multi stage filter bank in VHDL and synthesized in the XILINX FPGA-S6LX9 and shown the comparison in terms of area, power and delay reports.

Existing System:

Recently, mobile communications has to ensure a wide frequency band to transmit a large amount of data with a high data rate. It is evolving into advanced communications such as LTE (4G services) to realize large amounts of data and fast transmission speed, and now has 5G mobile communications in the spotlight. Therefore, spectrum allocation for mobile communications is becoming increasingly complicated. In base stations and repeaters, spectrum efficiency is maximized by using filters to minimize the interference of adjacent frequencies. The filters are employed to suppress crosstalk between adjacent signals, to minimize interference between transmission and reception frequencies, and to suppress spurious emissions caused by inter modulation in the system.

General base stations and repeaters in mobile communications adopt super-heterodyne receivers, which eliminate adjacent bands at intermediate frequency (IF). This system generally utilizes analogue IF band pass filters to minimize various frequency interference between heterogeneous services, adjacent service providers, and transmission and reception. These analog filters include an LC filter and a surface acoustic wave (SAW) IF filter. Recently, SAW filters have been replaced with digital IF filters based on finite impulse response (FIR). The SAW filter has high frequency stability and selectivity. However, when repeaters and base stations want to change the center frequency and bandwidth for new service adaptation, a new SAW filter should be developed and embedded due to its fixed frequency characteristics. As a result, system development is needed for the changed frequency environment or is supposed to adopt multiple SAW filters of two or more types, which causes both the increase of system costs and the delay in service opening. For these reasons, development of a variable digital filter responding to changeable frequency environments is required.

Variable digital FIR filters have been researched to be applied to various specifications of application services. Therefore, in this brief, we propose a reconfigurable digital IF filter that can adjust both the center frequency and bandwidth while maintaining high frequency selectivity as an existing fixed SAW filter. Since the digital band pass filter of IF band needs to support high sampling rate, a large number of taps are required for high frequency selectivity, which results in increasing hardware complexity significantly. Various digital FIR structures with low complexity have been proposed. According to this tendency, in this brief, we propose a filter bank lowering the sampling rate in order to reduce the hardware complexity of a single digital band pass filter. In addition, we also propose a band pass filter with a recursive multi-stage structure working at a lower sampling rate.

Disadvantages:

- The existing SAW filters does not have the variable centre frequency, it only has a fixed frequency.
- SAW filters produces the more delay in service openings.

Proposed System:

Due to limited frequency resources, new services are being applied to the existing frequencies, and service providers are allocating some of the existing frequencies for newly enhanced mobile communications. Because of this frequency environment, repeater and base station systems for mobile communications are becoming more complicated, and frequency interference caused by multiple bands and services is getting worse. The IF (Intermediate Frequency) Filters with high selectivity is used to reduce the interference between the different frequency range. Therefore, the heterodyne receivers uses the IF filter. In mobile communication the repeaters and the base station cannot actively cope because, it has fixed frequency range. Therefore, this paper proposes the new design concept of low complexity and efficient reconfigurable digital IF filters using multi stage filter bank. The multi stage filter bank of the proposed digital IF filters lowering the sample rate in order to reduce the hardware complexity. The existing system of digital IF filters uses the concept of SAW(surface acoustic wave) IF filter, it has high frequency stability and selectivity but, it does not have variable centre frequency. The SAW IF filters has the fixed frequency level only. Therefore the proposed system of digital IF filters uses the concept of multi stage filter bank in order to reduces the hardware complexity and better performance. The proposed digital IF filters uses the different centre frequency from the range of 500MHZ to 1GHZ and filter bandwidth can be selective to one of 10MHZ, 15MHZ and 20MHZ frequency level. The proposed digital IF filter reduces the complexity of adders and multipliers. Finally, The Digital IF filter using multi stage filter bank in VHDL and synthesized in the XILINX FPGA-S6LX9 and shown the comparison in terms of area, power and delay reports.

Digital IF Filter System

A digital FIR filter can change its center frequency and bandwidth by adjusting filter coefficients. In this brief, we design a digital IF filter that sets coefficients from a software to change both the center frequency and the bandwidth. Since the hardware structure is likely to be fixed and has less flexibility,

Table 1: Specification of IF Filter

Item	Unit	MIN	TYP	MAX
Center frequency	MHz	-	62.5	-
Bandwidth	MHz	9.015		18.44
40 dB Bandwidth	MHz	11.6		21.6
Ultimate Rejection	dBc	40		
Insertion Loss	dB			10
ACRR[a]	dBc		20	
EVM[b]	%			8

a-Adjacent channel rejection ratio

b -Error vector magnitude

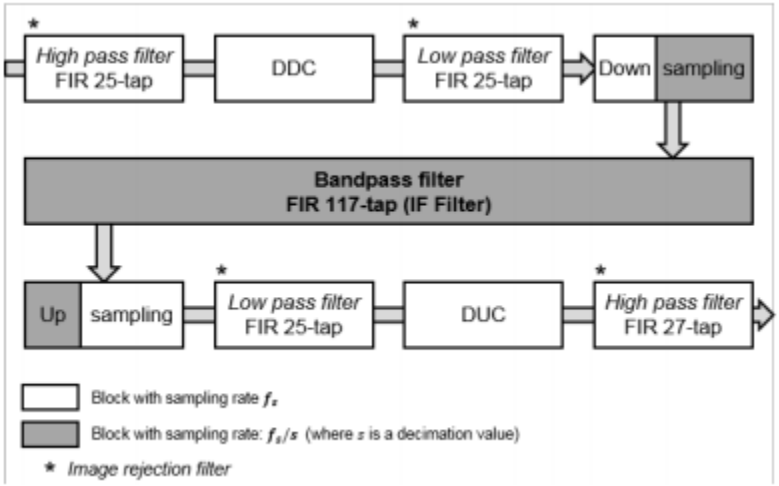

Figure 1: Digital IF Filter Using Filter Bank

the maximum number of taps has to be determined first. The maximum number of taps can be given from the required frequency response of filter, which is a function of a sampling rate, transition width (frequency gap between the end of pass band and the start of stop band), ripple in the pass band, and suppression in the stop band. In this brief, we design a filter depending on the specification of Table I according to the ITU standards required for 3G and 4G mobile communication systems. The maximum number of taps needed in the filter can be obtained by using the MATLAB Filter Design & Analysis (FDA)

tool. Since the required number of taps increases in proportion to the sampling rate, the maximum number of taps is given at the highest center frequency of IF band.

The digital IF filter requires a large number of taps, because the filter has to meet the specifications in Table while working at a high sampling rate for high frequency selectivity. This causes the hardware resources of filter more complex. Therefore, in order to reduce the hardware complexity of filter, we propose both a filter bank structure using a digital down converter (DDC) and a digital up-converter (DUC) and a band pass filter structure using a multi-stage scheme.

Filter bank with a DDC and a DUC

In order to reduce the hardware complexity of digital IF filter, simple approach is to decrease sampling rate, this makes a filter bank structure adopt a DDC and a DUC. Since the number of taps highly depends on the sampling rate, to have the sampling rate lower at the same bandwidth is to reduce the complexity of filter effectively. The filter bank consists of a DDC, decimation (down sampling), and interpolation (up sampling),

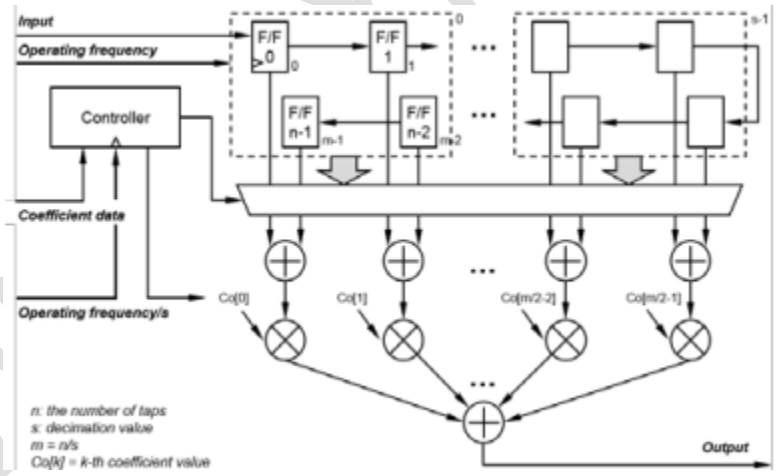

Figure 2: Digital band pass filter with Multi stage in Filter bank

and a DUC. It includes four image rejection filters (IRFs) to reject images that occur during down-conversion or up conversion. As shown in above Figure prior to the band pass FIR filter, there are the DDC to lower the center frequency and decimation to reduce sampling rate, $ffss$. As the sampling rate

is lowered due to the decimation process, $ffss/ss$, the same filter performance can be achieved with fewer taps than an existing single digital filter. After band pass filtering, up sampling is performed to recover the sampling rate, $ffss$, and the center frequency is moved to the original position through the DUC. Four IRFs with a few taps have to be deployed both before and after the DDC and DUC to remove images.

For the same frequency response of filter, the number of taps (N) can be decreased to N/s by reducing the sampling rate to 1/s in decimation. Because of digitized down-converting, however, the decimation value, s, in the proposed system has to have a natural value and be limited by several system parameters such as IF carrier frequency and bandwidth in commercial repeaters. A digital IF filter has to works in the given IF carrier frequency (from 10MHz to 65MHz), which has been generally used for

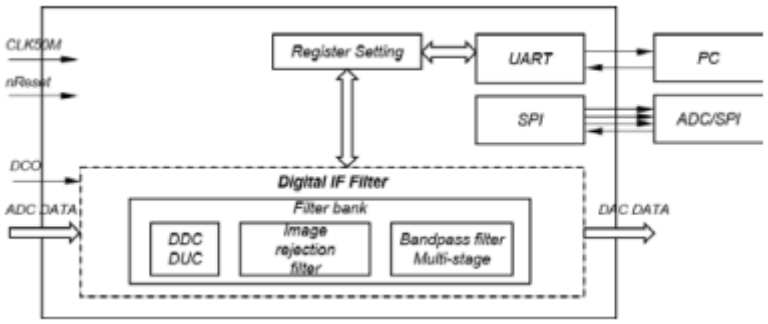

Figure 3: Block diagram of digital IF filter

analog IF SAW filters in commercial repeaters. For the given sampling rate and bandwidth, s is obtained, and then the optimized BPF can be designed for specifications required in the standard. For each IRF, the minimum number of taps is estimated in MATLAB simulation in order only to reject images. Since the filtered data of BPF is not corrupted through the image rejection process and the desired data are far away from images, the required number of taps for IRFs in the filter bank is very small as shown in Figure. The low cost paid for IRFs makes the total number of taps effectively reduced. In this approach, the complexity of proposed filter can be reduced considerably.

We use the MATLAB FDA tool to generate the coefficient of filters in the proposed filter bank for the specifications given in Table. The complexity of proposed filter using a filter bank can be reduced by 16.42% and 19.85% with respect to the number of multipliers and the adders, respectively, compared with the single digital filter without a filter bank.

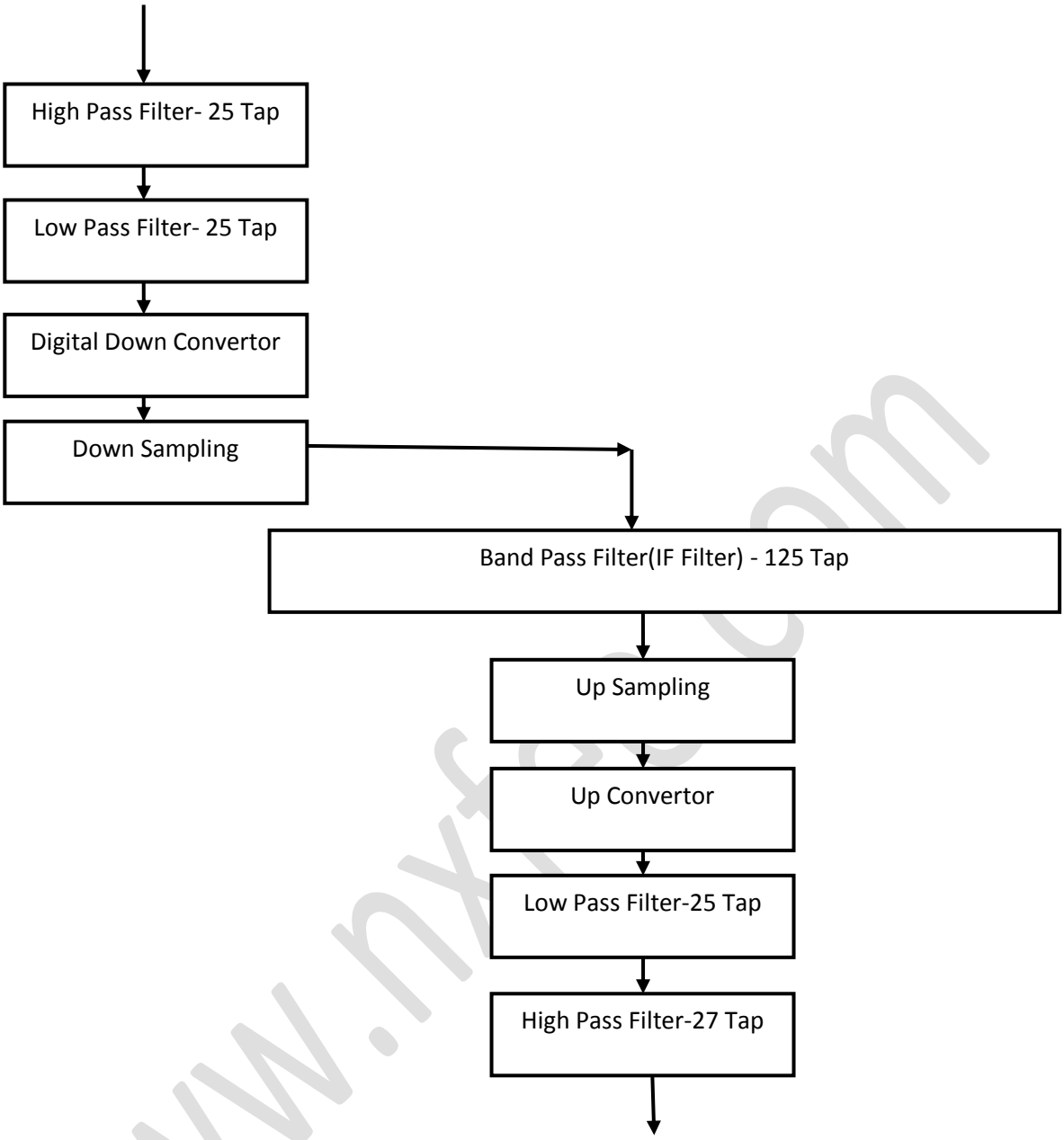

Figure 4: Block Diagram of the proposed IF filter using multi stage filter bank.

Digital IF band pass filter with multi-stage structure

In the band pass filter, which is a digital FIR filter working at the down sampling rate, it is possible to perform parallel operation when maintaining the original clock speed even after decimation process. The above Figure shows a block diagram of the proposed multi-stage structure. In the proposed multi-stage structure, the original structure of FIR filter is divided into s same structures by the ratio of

decimation, s. The original n order FIR filter requires n-1 adders and n/2. When the data stream is decimated by the ratio of s, the speed of data fed into the filter is also reduced to one-s-th. The regular filter unit with 1/s adders and 1/s multipliers can perform the same work as the original n-order FIR filter by repeating filter operation s times recursively at the original working speed. With this approach, both the number of adders and multipliers can be reduced by 1/s compared to an existing band pass FIR filter without a multistage structure.

The number of multipliers and adders of an existing single IF filter and the proposed IF filter using both the filter bank and the multi-stage structure. When s is 2, the hardware costs of multipliers and adders are reduced by 38.81% and 41.57%, respectively. The reduction ratio of proposed IF filter is higher in terms of hardware costs when the multi-stage structure is employed compared to the filter bank structure.

Advantages:

- IF Filter is used to minimize the interference between the frequencies.
- The IF Filters with variable centre frequency and bandwidth achieves high selectivity.
- The filter bank lowering the sample rate in order to reduce the hardware complexity.

Literature Survey:

- Z. Shen, A. Papasakellariou, J. Montojo, D. Gerstenberger, and F. Xu, "Overview of 3GPP LTE-advanced carrier aggregation for 4G wireless communications." IEEE Communications Magazine 50, no. 2 (2012). -To satisfy the ever increasing demand for higher throughput and data rates, wireless communication systems need to operate in wider bandwidths. 3GPP LTE-Advanced with carrier aggregation enables operators to maximally and optimally utilize their available spectrum resources for increased data rates and user experience while reducing their incurred OPEX and CAPEX. This article provides a tutorial overview of 3GPP LTE-Advanced with carrier aggregation as specified in Rel-10 including deployment scenarios of interest, main design features, PHY/MAC procedures, and potential enhancements for future standard releases.

- D. B. Chester, "Digital IF filter technology for 3G systems: An introduction." IEEE communications magazine 37, no. 2 (1999): 102-107-Contemporary digital communication systems such as those being developed for the deployment of third-generation cellular require ever increasing

performance levels in their signal processing chains to extract higher data rates and to provide decreasing price/performance ratios. Additionally, communication systems like 3G that must support multimode flexibility, such as the software radio, must be able to reconfigure their signal processing chains while keeping circuit complexity to a minimum. Given these constraints, DSP is the only viable alternative for baseband processing and digital IF processing. DSP is in many cases the only viable alternative to analog IF processing. Digital IF affords greater flexibility and higher performance in terms of attenuation and selectivity. It also offers better time and environment stability and lower equipment production costs than traditional analog techniques.

- Mehrnia, M. Dai, A. N. Willson, "Efficient halfband FIR filter structures for RF and IF data converters." IEEE Transactions on Circuits and Systems II: Express Briefs63, no. 1 (2016): 64-68- Halfband filters used in multi-gigasample-per-second radio frequency/intermediate frequency data converters to interpolate or decimate the signal are responsible for a considerable portion of the power consumption. We now know that the sensitivity of halfband filters to coefficient quantization can be systematically reduced. This can be exploited in the filter-design process to yield halfband filters with reduced hardware complexity, leading to lower power consumption and/or higher operating speeds. The general derivation of such desensitized halfband structures and the relationship between their coefficients and those of conventional halfband filters are presented. Cadence implementation results show significant improvements.

- G. Fischerauer, T. Ebner, P. Kruck, K. Morozumi, R. Thomas, and M. Pitschi, "SAW filter solutions to the needs of 3G cellular phones." In Microwave Symposium Digest, 2001 IEEE MTT-S International, vol. 1, pp. 351-354. IEEE, 2001- Services based on third-generation (3G) cellular phone standards like W-CDMA or cdma-2000 will be launched in the very near future. They will bring together mobile telephony and applications such as internet communication, digital picture transmission or video conferencing that require high data rates. This objective and other provisions in the new standards lead to significantly changed requirements on the surface acoustic wave (SAW) filters employed in the IF and RF stages of 3G cell phones when compared to second-generation (2G) systems. The present contribution discusses the main issues involved in the design of SAW filters for 3G cell phones, with an emphasis on W-CDMA. The key point is that the need for miniaturization, higher operating frequencies and improved performance can

only be met by a proper choice of material system, filter technique and package technology. In particular for the RF filters, it is essential to include in the simulation model a correct electrical description of the miniaturized package. State-of-the-art examples serve to illustrate these points.

- K.-H. Chen and T.-D. Chiueh, “A low-power digit-based reconfigurable FIR filter,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 8, pp. 617–621, Aug. 2006-In this brief, we present a digit-reconfigurable finite-impulse response (FIR) filter architecture with a very fine granularity. It provides a flexible yet compact and low-power solution to FIR filters with a wide range of precision and tap length. Based on the proposed architecture, an 8-digit reconfigurable FIR filter chip is implemented in a single-poly quadruple-metal 0.35-mum CMOS technology. Measurement results show that the fabricated chip operates up to 86 MHz when the filter draws 16.5 mW of power from a 2.5-V power supply.

- S. Dhabu, and A. P. Vinod, "Design and FPGA Implementation of Reconfigurable Linear-Phase Digital Filter With Wide Cutoff Frequency Range and Narrow Transition Bandwidth." IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 63, no. 2, pp. 181-185, 2016 -Reconfigurable filters based on the spectral parameter approximation (SPA) technique and its combination with other techniques provide a continuous control over the cutoff frequency (f_c). However, when very wide f_c range and narrow transition bandwidth is desired, these filters either fail to satisfy some of the specifications or have extremely high complexity. In this brief, we propose an interpolated SPA (ISPA) filter that overcomes all the limitations of all the existing SPA technique based filters, and achieves very wide f_c range (equal to approximately the entire Nyquist band) and narrow transition bandwidth along with small passband ripple and high stopband attenuation. Comparison with the state-of-the-art reconfigurable filters is provided via a design example, which shows that the ISPA filter achieves more than 50% savings in the number of multipliers compared to the filter based on the combination of SPA and modified coefficient decimation techniques. The field-programmable gate array implementation results show that the ISPA filter has much lesser group delay and much higher operating speed, but incurs moderate penalty in terms of area compared to the filter based on the combination of frequency transformation and interpolation techniques.

- K. Mohanty, and P. K. Meher. “A high-performance FIR filter architecture for fixed and reconfigurable applications.” IEEE transactions on very largescale integration (vlsi) systems 24, no. 2 (2016): 444-452-Transpose form finite-impulse response (FIR) filters are inherently pipelined and support multiple constant multiplications (MCM) technique that results in significant saving of computation. However, transpose form configuration does not directly support the block processing unlike direct-form configuration. In this paper, we explore the possibility of realization of block FIR filter in transpose form configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications. Based on a detailed computational analysis of transpose form configuration of FIR filter, we have derived a flow graph for transpose form block FIR filter with optimized register complexity. A generalized block formulation is presented for transpose form FIR filter. We have derived a general multiplier-based architecture for the proposed transpose form block filter for reconfigurable applications. A low-complexity design using the MCM scheme is also presented for the block implementation of fixed FIR filters. The proposed structure involves significantly less area-delay product (ADP) and less energy per sample (EPS) than the existing block implementation of direct-form structure for medium or large filter lengths, while for the short-length filters, the block implementation of direct-form FIR structure has less ADP and less EPS than the proposed structure. Application-specific integrated circuit synthesis result shows that the proposed structure for block size 4 and filter length 64 involves 42% less ADP and 40% less EPS than the best available FIR filter structure proposed for reconfigurable applications. For the same filter length and the same block size, the proposed structure involves 13% less ADP and 12.8% less EPS than that of the existing direct-form block FIR structure.

- Surface acoustic wave (SAW) filters of assessed quality - Part 1: Generic specification, IEC 60862-1:2003 Standard, May 19, 2003 -IEC 60862-1:2015 specifies the methods of test and general requirements for SAW filters of assessed quality using either capability approval or qualification approval procedures. This edition includes the following significant technical changes with respect to the previous edition: 1. the terms and definitions from IEC 60862-2:2002 are included; 2. the measurement method for the balanced type filter is described; 3. the electrostatic discharge (ESD) sensitivity test procedure is considered.

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[6] S. Dhabu, and A. P. Vinod, "Design and FPGA Implementation of Reconfigurable Linear-Phase Digital Filter With Wide Cutoff Frequency Range and Narrow Transition Bandwidth." IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 63, no. 2, pp. 181-185, 2016

[7] B. K. Mohanty, and P. K. Meher. “A high-performance FIR filter architecture for fixed and reconfigurable applications.” IEEE transactions on very largescale integration (vlsi) systems 24, no. 2 (2016): 444-452.

[8] 3GPP TS36.106, “FDD repeater radio transmission and reception”

[9] Surface acoustic wave (SAW) filters of assessed quality - Part 1: Generic specification, IEC 60862-1:2003 Standard, May 19, 2003

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[11] Oscilent Corporation, "PRODUCT SPECIFICATION; 62.5 MHz IF SAW Filter 19.62 MHz Bandwidth (809-SL62.5M-19C)"

[12] 3GPP TR25.956, “UTRA repeater planning guidelines and system analysis”